Attorney Docket No. 24096.00300/00SC003

PATENT APPLICATION

HIGH GAIN DETECTOR AMPLIFIER WITH ENHANCED DYNAMIC RANGE FOR SINGLE PHOTON READ-OUT OF PHOTODETECTORS

Inventors: Lester J. Kozlowski

William E. Tennant

Assignee: Rockwell Technologies, LLC

Crosby Heafey Roach & May
P.O. Box 7936
San Francisco, CA 94120-7936
(415) 543-8700

HIGH GAIN DETECTOR AMPLIFIER WITH ENHANCED DYNAMIC RANGE FOR SINGLE PHOTON READ-OUT OF PHOTODETECTORS

BACKGROUND OF THE INVENTION

Ins. A1

The present application is related to U.S. Patent Application Serial No. _____, entitled "SELF-ADJUSTING ADAPTIVE MINIMAL NOISE INPUT AMPLIFIER", attorney docket number 24096.00800/00SC004, filed September 29, 2000; and is also related to U.S. Patent Application Serial No. _____, entitled "ADAPTIVE AMPLIFIER CIRCUIT WITH ENHANCED DYNAMIC RANGE", attorney docket number 24096.00900/99SC026, filed September 29, 2000, the disclosures of which are herein incorporated by reference.

1. Field of the Invention

This invention relates to ultra-low noise photon detection in low-light-level conditions and, specifically, to low-noise, high-gain, wide dynamic range pixel amplifiers with high bandwidth for single photon readout of various photodetectors in imaging arrays.

2. Description of the Related Art

Optical sensors transform incident radiant signals in the X - ray (λ<0.001μm), ultraviolet (λ=0.001 - 0.4μm), visible (λ=0.4 - 0.8μm), near infrared (IR) (λ=0.8 - 2μm), shortwave IR (λ=2.0 - 2.5μm), mid IR (λ=2.5 - 5μm), and long IR (λ=5 - 20μm) bands into electrical signals that are used for data collection, processing, storage and display, such as real-time video. Available conventional photodetectors such as photodiodes and photoconductors are inexpensive, exhibit bandwidths that support current video frame rates, are sensitive to wavelengths well into the long IR band, and exhibit a high degree of uniformity from pixel to pixel when used in an imaging array. However, these photodetectors have no gain, i.e. each incident photon generates, at most, a single electron. Thus, these imaging systems work well only in moderate to bright light conditions. At low light levels,

they provide electrical signals that are too small to be read-out by conventional readout circuits.

In conditions of low ambient light, the standard photodetector is often replaced with an avalanche photodiode that provides significant gain such that conventional read-out circuits, such as charge coupled devices, i.e. CCDs, can read out the amplified signal at video frame rates with a high signal-to-noise ratio (SNR). The fabrication of avalanche photodiodes is much more difficult and expensive than standard photodetectors because they must simultaneously exhibit very high controlled gain and very low noise. Furthermore, currently available avalanche photodiodes exhibit relatively poor uniformity, are constrained to shorter wavelengths than standard photodetectors (0.7μm), and have limited sensitivity due to their relatively low quantum efficiency. Imaging intensified systems use an array of avalanche photodiodes or micro-channel plates to drive respective display elements such as CCDs or phosphors, and have even lower wavelength capabilities (approximately 0.6μm max) due to the limitations of the photodiode.

Chamberlain et al. "A Novel Wide Dynamic Range Silicon photodetector and Linear Imaging Array" IEEE Transactions on Electron Devices, Vol. ED-31, No. 2, February 1984, pp. 175 - 182, herein incorporated by reference, describes a gate modulation technique for single photon read-out of standard photodetectors with wide dynamic range. Chamberlain provides a high-gain current mirror that includes a load FET (Field Effect Transistor) whose gate is connected to its drain to ensure sub-threshold operation. The signal from the photodetector is injected into the load FET thereby producing a signal voltage at the gate of a gain FET with high transconductance. This signal modulates the gain FET's gate voltage, which is read out and reset via a FET switch. The key benefit of this approach is that a detecting dynamic range of more than 10^7 for each detector in the array is produced. Unfortunately, the circuit is highly sensitive to variations in the threshold voltage of the

various transistors. The pixel-to-pixel V_T non-uniformity associated with standard silicon CMOS fabrication processes degrades the instantaneous dynamic range of the imaging array even as the circuit's logarithmic characteristic enhances each pixel's ability to operate over a much larger total dynamic range.

Although this specific gain modulation technique is useful for detecting signals across a broad spectral range, the front-end bandwidth severely restricts the imaging array's bandwidth. Specifically, the dominant RC time constant is the parallel combination of the photodetector's capacitance and the resistance of the load FET. In sub-threshold operation, the FET's transconductance is very low and, hence, its load resistance is very large, at $\geq 10^{15}$ ohms; the minimum resulting RC time constant is on the order of tens of seconds. Chamberlain's gate modulation technique is thus only practically useful for imaging daylight scenes or static low-light-level scenes such as stars. Furthermore, to achieve large current gain, the load FET is typically quite small. As a result, the load FET exhibits substantial 1/f noise, which under low light conditions seriously degrades the performance of the imaging array.

U.S. Patent No. 5,933,190 discloses a circuit having a first reading transistor 23 in series with the load transistor of Chamberlain to read-out the voltage across the load transistor rather than the other leg of the current mirror. While this configuration self-biases the detectors in the imaging array, and the usable dynamic range for each pixel is still at least 10^7, the time constant is unchanged relative to Chamberlain's teaching. Further, the instantaneous dynamic range at a specific irradiance across an imaging array having pixels of such design is still highly sensitive to the threshold uniformity from transistor to transistor. The pixel-to-pixel V_T non-uniformity associated with standard silicon CMOS fabrication processes degrades the instantaneous dynamic range of the imaging array even as the circuit's logarithmic characteristic enhances each pixel's ability to operate over a much larger total

dynamic range. Though the '190 reference also teaches a method for reducing the non-uniformity by degrading the various transistors by applying a stressing over-voltage, this is definitely not a recommended procedure for a high-quality, long-life camera system.

U.S. Patent No. 5,929,434 teaches an alternative current mirror configuration that suppresses the impact of the V_T non-uniformity via an alternative current mirror configuration that also reads the integrated current after an integration period rather than the instantaneous voltage. The preferred embodiment minimizes, to first order, the variations in threshold non-uniformity by subtracting the non-uniformity within each pixel. Unfortunately, the pixel-to-pixel variations still dominate the imager's fixed pattern noise irrespective of background flux, depending on the MOS fabrication technology. Such pattern noise can often be larger than the signal.

The negative feedback amplifier, A1, disclosed in 5,929,434, significantly reduces the input impedance of the high-gain circuit and thereby enhances its bandwidth. In the case where the buffer amplifier is approximated to have infinite voltage gain and finite transconductance, the dominant pole is given by:

$$\tau_{B-L} = \frac{C_f}{g_{m_{Q1}}}$$

where C_f is the effective feedback capacitance of the buffer amplifier from its output to its input. Assuming a cascoded amplifier configuration, the gate-source capacitance of Q1 is dominant and C_f is set by the gate-to-source capacitance of the sub-threshold FET Q1. This is approximately given by the parasitic metal overlap capacitance. Assuming a minimum width transistor in 0.25μm CMOS technology, for example, the minimum C_f will be approximately 0.2 fF for transistors having minimum width. The resulting time constant is on the order of tenths of a second. Though this facilitates single photon sensing at roughly video frame rates, additional improvements are needed to truly support single-photon imaging.

U.S. Patent No. 5,665,959 teaches yet another approach consisting of a digitized system wherein each pixel uses a pair of cascaded inverters with a sub-threshold transistor at its front-end to generate extremely high transimpedance. Since the small photosignal at backgrounds on the order of one electron translates to extremely high input impedance, the photosignal is effectively integrated onto the Miller capacitance of a first-stage inverter prior to being further amplified by a second stage inverter. A resulting charge-to-voltage conversion gain >1 mV/e- is hence claimed. Nevertheless, the read noise of the charge-integrating first stage will limit the SNR for many practical cases since insufficient means are provided to band-limit the first amplifier's wideband noise. The read noise for the first stage can be approximated as similar to that of a charge integrator such that:

$$N_{stage\_1} = \frac{1}{q}\sqrt{kTC_{fb}\cdot\frac{C_{\det}+C_{fb}}{C_L+\frac{C_{fb}\cdot C_{\det}}{C_{fb}+C_{\det}}}}$$

where k is Boltzmann's constant, T is the temperature, C_{fb} is the parasitic feedback capacitance of the first stage, C_{det} is the photodiode capacitance and C_L is the load capacitance at the amplifier's output. Assuming practical values consistent with the understanding of those skilled in the art, the detector capacitance is typically a minimum of 15 fF for the hybrid imager of the 5,665,959 preferred embodiment. Assuming a Miller capacitance for the first stage amplifier of 5 fF and a load capacitance of 350 fF (i.e., the storage capacitance C_{str1}), then the minimum read noise for the first stage will be in the range of 6 to 7 e-; this is on top of the kT/C noise generated by opening transistor switch Q_{SW1} to perform the offset compensation of the composite two-stage amplifier. This performance is very good, but does not facilitate photon counting. Further, while the clocking of the two-stage amplifier

facilitates large reductions in amplifier non-uniformity, this invention does not suppress the threshold variations of the load resistor at the front end.

SUMMARY OF THE INVENTION

In general, the present invention provides an ultra-low noise, high-gain pixel amplifier to facilitate single-photon read-out across the electromagnetic spectrum from the x-ray to long IR bands at video frame rates and higher. The present invention supports various types of high impedance detectors, both photovoltaic and photoconductive, and generates minimum fixed pattern noise.

More particularly, the present invention is an adaptive detector amplifier circuit comprising a high-gain detector interface with self-nulling offset suppression to simultaneously provide high gain, low offset non-uniformity and wide dynamic range. The front-end provides both high gain and wide signal bandwidth by integrating the photocharge on the detector's capacitance. The front-end also facilitates extremely low read noise by using a feedback-enhanced reset amplifier to suppress the kTC noise below 1 e-. The integrating photocharge modulates a current source whose gain-proportioned signal may be integrated during the entire integration time or for only a fraction of the integration time, at the operator's choice. This gain is adjustable, varying exponentially with gain voltage and can be set appropriately larger at small signal levels to enable sub-electron read noise even in the presence of the kTC noise of the integration capacitor.

Since the current required for high gain will be large and since variations in the threshold voltage of the modulated transistor would normally generate large non-uniformity in these large currents, the present invention incorporates an adaptive skimming circuit at the back-end to minimize the signal non-uniformity. Though the present circuit can be readily configured as an integrator with a rolling-type electronic shutter, synchronous image formation (snapshot) is facilitated by appropriately applying a global reset clock rather than a rastered reset clock. This function separates signal integration on the diode from the gain-proportioned assimilation on an integration capacitor, C_{int}. This requires the gain to be set

high enough to allow the charging of C_{int} in a small fraction of the frame time. If desired, a more conventional snapshot circuit with a second integration capacitor can also be employed. Additionally, one embodiment of the present invention includes a source-follower amplifier at the pixel's output to buffer the signal read through the bus. This amplifier may not be necessary if the charge integrated in the cell is large enough.

The present solution can be integrated into the typical pixel pitches normally used for single-photon detection (from 40μm to 125μm) to amplify only the noise-free photo-generated signal for subsequent processing or display. The resulting video signal has large margin over the background noise of the camera electronics even at very low levels of ambient light without need for supplementary illumination.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

Figure 1 is a schematic diagram of a first embodiment of an ultra-low noise, high gain, high-bandwidth pixel amplifier for single-photon readout of various photodetectors with either snapshot or focal-plane-shutter image formation;

Figure 2 is a schematic diagram of a second embodiment of an ultra-low noise, high gain, high-bandwidth pixel amplifier for single-photon readout of various photodetectors with either snapshot or focal-plane-shutter image formation;

Figure 3 is a schematic diagram of a third embodiment of an ultra-low noise, high gain, high-bandwidth pixel amplifier for single-photon readout of various photodetectors with preference for focal-plane-shutter rather than snapshot imager formation and compatibility with smaller pixel pitch; and

Figure 4 is a schematic diagram of a CMOS inverter amplifier of the various embodiments for facilitating low noise detector reset via capacitive feedback.

DETAILED DESCRIPTION OF THE INVENTION

The following description is provided to enable any person skilled in the art to make and use the invention and sets forth the best modes contemplated by the inventors for carrying out the invention. Various modifications, however, will remain readily apparent to those skilled in the art, since the basic principles of the present invention have been defined herein specifically to provide a low-noise, high-gain, wide dynamic range pixel amplifier with high bandwidth for single photon readout of various photodetectors in imaging arrays. Any and all such modifications, equivalents and alternatives are intended to fall within the spirit and scope of the present invention.

The present invention provides a high bandwidth, ultra low-noise pixel amplifier that is capable of single photon read-out of photodetectors in extremely low-light conditions, i.e. photon flux levels approaching zero photons per sampling period. This circuit can be used to effectively count incident photons on individual photodetectors, in an imaging array as the front-end to a conventional video system, or in high frame-rate wavefront sensors. One of the primary benefits of the present approach is that the circuit can use "off-the-shelf" photodetectors such as photodiodes or photoconductors that have gain ≤ 1 rather than, for example, avalanche multiplication within the photodiode (avalanche photodiodes). Standard photodetectors with gain ≤ 1 are cheaper, more uniform, easier to fabricate, more reliable, less susceptible to excess noise mechanisms within the detector, and support a much broader range of the electromagnetic spectrum than avalanche photodiodes.

Figure 1 is a schematic of a first embodiment of the present invention. The left-most portion of the circuit 2 is a reset amplifier 4 that is implemented as a CMOS inverter. To

reset the detector PD1, the amplifier 4 is enabled along with the reset transistor Q41. Negative feedback in conjunction with the small feedback capacitance of the amplifier's Miller capacitance and a large load capacitance C_L (both internal and external to the pixel) nearly eliminate the kTC noise otherwise generated. Using an amplifier transistor of three to four times the minimum feature size in 0.25μm CMOS technology effects a sub-1fF Miller capacitance. Combining in parallel the in-cell C_L with both the load bus capacitance and other capacitance external to the cell readily enables total load capacitance of 5 pF. Conservatively assuming a detector capacitance of 50 fF and substituting into the earlier equation for a reset integrator yields a residual reset noise of approximately 1 electron. The operation of the basic CMOS inverter is described below with reference to Figure 4.

The rightmost portion of the circuit 2 is a high-gain read amplifier 6. After reset is completed the reset amplifier 4 is disabled and detector charge is allowed to integrate on the detector capacitance. The integrating signal modulates the gate of a current source transistor Q61 whose gain-proportioned current is integrated in the integration capacitor C_{int} (part of the adaptive skimming circuit 8) for a programmed integration time. The integration capacitor C_{int} is preferably formed from a MOSFET, with its source and drain connected. This integrated signal, whose Nyquist-limited noise is dominated by the shot noise of the amplified photosignal can thus be directly read to the bus or through an optional source follower Q24 bus.

As explained in more detail in U.S. Patent Application Serial No. _____ , entitled "SELF-ADJUSTING ADAPTIVE MINIMAL NOISE INPUT AMPLIFIER", attorney docket number 24096.00800/00SC004, filed September 29, 2000, herein incorporated by reference, the non-uniformities in the integrated current are subtracted from the amplified signal pedestal by operation of the adaptive skimming circuit 8.

Though image formation is typically of a rolling-shutter or focal-plane-shutter type, snap-shot integration may be achieved by sampling the voltage accumulated on C_{int} onto $C_{S/H}$ by enabling $\phi_{S/H}$ (on the sample-and-hold transistor Q65). The imaging array is subsequently reset synchronously by enabling ϕ_{pix_reset} (on the pixel reset transistor Q64) to reset C_{int} and ϕ_{rst_Det} (on the detector reset transistor Q41) to reset the detector PD1. Since the front-end circuit 4 is a logarithmic amplifier, the integrator should be disabled during the reset processes. Therefore, V_{Gain} should be disabled to prevent signal integration during reset.

Also, to facilitate snap-shot integration an additional current source CS1 may be added to each pixel cell. If snap-shot functionality is not needed, then this current source CS1 can be removed from each cell and a single current source placed on the common bus, in order to reduce the area of each pixel.

Figure 2 is a schematic of an alternative embodiment of the present invention. In this circuit 10, the charge integrator used to reset the detector PD1 provides an autozero feature to eliminate the programming of the amplifier offset non-uniformity onto the detector voltage. This is accomplished via the autozero transistor Q101, and the combination of $C_{autozero}$ and C_{fb}.

Figure 3 is a schematic of another alternative embodiment of the present invention. Here, the reset integrator is distributed between the pixel and an external circuit CS2 shared among all the pixels in a column. In this embodiment, the pixels must be reset on a row-by-row basis. While snapshot integration is still technically possible, rolling integration is preferred. By removing the potentially large C_L capacitor from the pixel, a smaller pixel pitch is now feasible.

A simple calculation of the SNR one would expect from the various embodiments of the photon-reading circuit is given by:

$$SNR = \frac{qN_p}{C_{\det}V_T}\sqrt{\frac{C_{\text{int}}V_{\max}}{rq}}$$

where C_{int} is the integration capacitance, V_{max} is the maximum useable output voltage, r is the skim reduction ratio, q is the electronic charge, N_p is the number of photogenerated charges on the diode, C_{det} is the diode capacitance, and V_T is the thermal voltage. For (in standard units) C_{int}=1pF, C_{det}=40fF, V_T=25mK, V_{max}=1V, and r=0.1, then

$$SNR = 1.26 \cdot N_p$$

The SNR is thus 1.26 when one photon is present. Sub-electron read noise is reduced by using high-gain front-end with a current-nulling backend to suppress the otherwise dominant threshold voltage non-uniformity.

In the single-ended CMOS inverter amplifier, shown separately in Figure 4, an input signal V_, whose voltage is more negative than was previously present, causes the p-MOSFET driver Q60 (Q44 of Figure 1) to conduct more strongly. In response, the amplifier's output voltage subsequently swings to a more positive potential since the load FET's (an n-MOSFET device Q62 (Q42 of Figure 1) whose nominal operating resistance is set by gate voltage V_{Gain}) relative operating resistance will be proportionally larger than before. An input signal V_ whose voltage is more positive causes the driver MOSFET Q60 to conduct less strongly; the resulting output voltage V_o thus swings again in a direction opposite to that of the input signal. The open-loop gain of this inverter is the product of the amplifier transistor's conductance, g_m, and the load resistance, r_d, established by the load transistor and the downstream load. The open-loop gain of the cascoded CMOS inverter amplifier configuration, where cascode transistor Q64 is inserted between the output node V_o and the drain of transistor Q60 is (for the case where p-MOSFET cascode transistor Q64 has identical geometry to the p-FET driver and is biased by gate voltage V_{Gain}):

$$A_v = -\left[\frac{g_m * r_d}{1 + \frac{r_d}{R_L}}\right] \qquad (1)$$

Where g_m is the transconductance of the amplifier transistor, r_d is the drain - source resistance of the load MOSFET and R_L is the load resistance at the amplifier output. Since this load is often purely capacitive for the intended application, i.e., the bus capacitance for the respective column or row of the imager, the denominator is often unity. In the absence of a cascode MOSFET, the gain is otherwise limited to $-g_m \cdot r_d$, as previously described.

Those skilled in the art will appreciate that various adaptations and modifications of the just-described preferred embodiments can be configured without departing from the scope and spirit of the invention. Therefore, it is to be understood that, within the scope of the appended claims, the invention may be practiced other than as specifically described herein.